**Standard Notations in FET:**

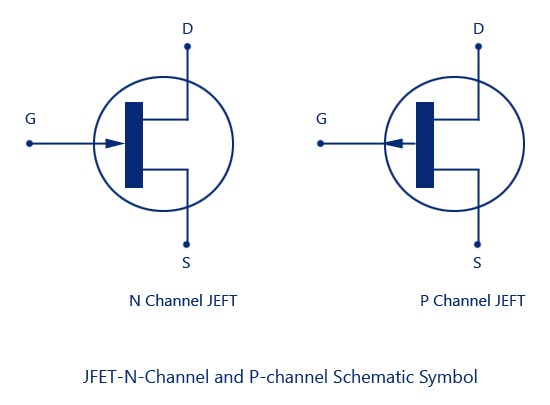
***Source –***The terminal through which the majority carriers enter the channel, is called the *source*terminal S and the conventional current entering the channel at S is designated as **I**g.

***Drain –***The terminal, througih which the majority carriers leave the channel, is called the *drain*terminal D and the conventional current leaving the channel at D is designated as ID.

The drain-to-source voltage is called VDS, and is positive if D is more positive than source S

***Gate –***There are two internally connected heavily doped impurity regions formed by alloying, by diffusion, or by any other method available to create two P-N junctions. These impurity regions are called the gate G. A voltage VGS is applied between the gate and source in the direction to reverse-bias the P-N junction. Conventional current entering the channel at G is designated as IG.

***Channel –***The region between the source and drain, sandwiched between the two gates is called the *channel*and the majority carriers move from source to drain through this channel.

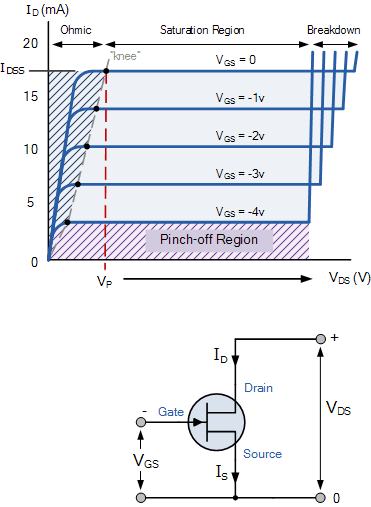
[](http://www.circuitstoday.com/wp-content/uploads/2009/08/JFET-N-Channel-and-P-channel-Schematic-Symbol.jpg)

## Applications of JFET

The **junction field effect transistor** has many application in the field of electronics and communication.  
Some of these applications are stated below.

1. Low noise and high input impedance amplifier:- Noise is an undesirable disturbance which interferes with the signals information - greater the noise less the information. Energy electronics device cause some amount of noise. If [FET](http://www.electrical4u.com/application-of-field-effect-transistor/) s is used at the front end, we get less amount of amplified noise at the output. Now, it has very high input impedance. So, it can be used in high input impedance amplifier.
2. **Buffer Amplifier:-** Buffer amplifier should have very high input impedance and low output impedance. Because of high i/p impedance and low output impedance, FET acts as great buffer amplifier. the common drain mode can be used in this purpose.
3. **R.F.Amplifier:-** JFET is good in low current signal operation as it is a voltage controlled semiconductors device. It has very low noise level. So, it can be used as RF amplifier in receiver sections of communication field.
4. **Current Source:-** Here all the supply voltage appears across load. If the current tries to increase very much, the excessive load a current drives the JFET in to active region. Thus JFET acts as a [current source](https://www.electrical4u.com/ideal-dependent-independent-voltage-current-source/).
5. **Switch:-** JFET may be used as an on/off switch controlling [electrical power](https://www.electrical4u.com/electric-power-single-and-three-phase/) to load. An example is given below

**Output characteristic V-I curves of a typical junction FET.**



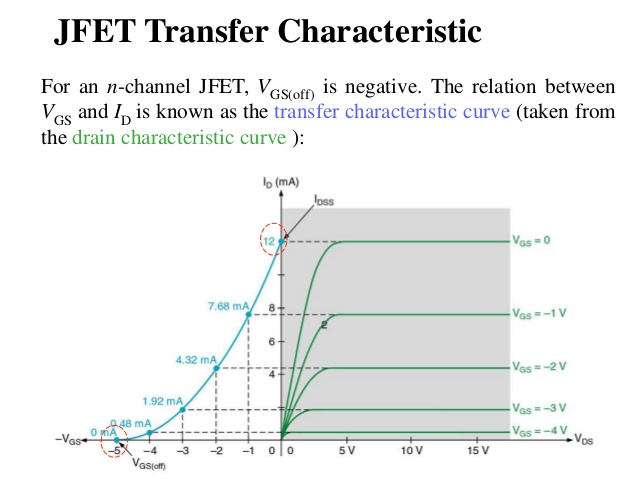
The voltage VGS applied to the Gate controls the current flowing between the Drain and the Source terminals. VGS refers to the voltage applied between the Gate and the Source while VDS refers to the voltage applied between the Drain and the Source.

Because a **Junction Field Effect Transistor** is a voltage controlled device, “NO current flows into the gate!” then the Source current ( IS ) flowing out of the device equals the Drain current flowing into it and therefore ( ID = IS ).

The characteristics curves example shown above, shows the four different regions of operation for a JFET and these are given as:

* Ohmic Region – When VGS = 0 the depletion layer of the channel is very small and the JFET acts like a voltage controlled resistor.
* Cut-off Region – This is also known as the pinch-off region were the Gate voltage, VGS is sufficient to cause the JFET to act as an open circuit as the channel resistance is at maximum.
* Saturation or Active Region – The JFET becomes a good conductor and is controlled by the Gate-Source voltage, ( VGS ) while the Drain-Source voltage, ( VDS ) has little or no effect.
* Breakdown Region – The voltage between the Drain and the Source, ( VDS ) is high enough to causes the JFET’s resistive channel to break down and pass uncontrolled maximum current.

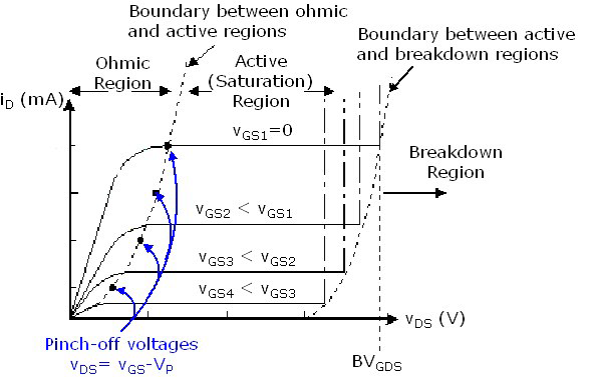
The characteristics curves for a P-channel junction field effect transistor are the same as those above, except that the Drain current ID decreases with an increasing positive Gate-Source voltage, VGS.

[](https://i.stack.imgur.com/h28Hc.jpg)

To the left is the transfer characteristic plotting Id against Vgs and to the right is the graph that shows the various conduction regions of the device.

The left hand plot is derived from the right hand plot by taking the points when Vds is at 10V (usually but not always) and translating across to the left hand graph so you get a plot of Id against Vgs.

Pinch off is where the device cross from being ohmic to saturating : -

[](https://i.stack.imgur.com/ILceR.png)

Maybe you are confusing this voltage with Vgs(off)?

SIGNIFICANT OF SLIP\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

Slip is a measure of the difference in relative motion between the rotor and the magnetic field set up by the field windings.  
  
In very simple terms, without **slip** an induction motor would not be able to develop any torque! A slip of zero means that the rotor is turning at synchronous speed; in other words it is running at the same speed as the rotating field set up by the field windings, so there is no relative movement between the field and the rotor. To develop torque, the voltages must be induced into the rotor, and this can only happen if there is relative movement between the field and the rotor -in other words, the rotor MUST be running more slowly than synchronous speed. That is, there must be some degree of slip.